AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph on page 4, lines 17-22 with the following:

A block schematic diagram of the preferred embodiment of the Iris Data Recovery Algorithm is depicted in Figure 2. A preamble detector circuit 100 receives an input signal V_{IN} and outputs an active preamble signal 112. A DC level set circuit~~signal~~ 200 receives the same input signal V_{IN} along with the preamble signal 112, a delay output 132 and a control signal V_C. The DC level set circuit 200 outputs a level set signal 300 to a data slicer circuit 400. The data slicer circuit 400 provides an output signal V_{OUT}.